Second Semester B. Sc. Examination

ELECTRONICS

Paper - II

(Advanced Digital Electronics)

Time : Three Hours] [Max. Marks : 50

N. B. : (1) All questions are compulsory and carry equal marks.
(2) Draw neat and well labelled diagrams wherever necessary.

EITHER

1. (A) Explain in detail, the construction and working of
(1) TTL NAND gate.
(2) C MOS NAND gate. 5+5

OR

(B) Elaborate the characteristics of digital logic families. Explain in detail the construction and working of TTL NOR gate. 5+5

EITHER

2. (A) Explain the function of PRESET and CLEAR in sequential logic with suitable diagram.
Elaborate the construction and working of JKMS flip-flop. 5+5

OR

(B) Draw the logic diagram of JKFF using NAND gates and explain its working. Discuss race around condition in JKFF along with timing diagram. How can it be minimise ? 5+5

EITHER

3. (A) What is a counter ? Define Asynchronous and synchronous counters. Elaborate the construction and working of 4-bit Johnson counter. Draw its timing diagram. 3+7

OR

(B) Define MOD of a counter. Describe working of a MOD-6 counter along with logic diagram, timing diagram and truth table. 2+8

EITHER

4. (A) What is a register ? State different types of shift register. Describe working of a 4-bit shift right register along with logic diagram, timing diagram and truth table. 3+7

OR

(B) What is a memory ? Elaborate classification of memory on the basis of speed. Construct 16x8K size memory block using 4x4k memory modules. 1+4+5

5. Solve any **ten** :—

(A) Define Tri-state logic.

(B) Define propagation delay.

(C) A TTL NAND gate is faster than CMOS NAND gate. State True or False.

(D) Define clock signal.

(E) Discuss positive and negative logic.

(F) State the advantages of edge - triggered over level triggered logic.

(G) Define ripple counter.

(H) State the application of a ring counter.

(I) State number of flip-flops required to construct MOD-4 counter.

(J) What is a volatile memory ?

(K) What is random access in a memory ?

(L) State number of memory modules of size 512x4 bits are required to construct memory of 2kx4 bits size. 1x10